**DOCKET NO. 00-C-050 (STMI01-00050)** **PATENT**
**Customer No. 30425**



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**



| | | |
|---|---|---|
| In re application of | : | William E. Ballachino |
| Serial No. | : | 09/667,164 |
| Filed | : | September 21, 2000 |
| For | : | M-BIT RACE DELAY ADDER AND METHOD OF OPERATION |
| Group No. | : | 2124 |
| Examiner | : | Chat C. Do |

**MAIL STOP PETITION**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

**DECLARATION OF KATHY A. HAMILTON**

I, Kathy A. Hamilton, declare:

1. My name is Kathy A. Hamilton. I am over the age of 18 and am competent to make this declaration. I have personal knowledge of the facts stated herein.

2. I am employed as a Legal Secretary by the law firm of DAVIS MUNCK, A Professional Corporation.

3. Attached hereto are copies of an Account Detail showing copying and postage charges for the above-identified application on October 7, 2003. Also attached hereto are copies of a postcard receipt, a Certificate of Mailing By First Class Mail, and a Response Under 37 C.F.R. § 1.111 (collectively "the Response documents").

4. My signature appears as the "Mailer" on the attached Certificate of Mailing By First Class Mail.

5. On October 7, 2003, I copied the originals for the Response documents as reflected by the copying charges in the attached Account Detail, then deposited the originals as "First Class Mail" with the United States Postal Service in an envelope with sufficient postage (as reflected by the postage charges in the attached Account Detail) addressed to MAIL STOP NON-FEE AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

6. All statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true. These statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon.

Date: Sept. 16, 2004

Kathy A. Hamilton

# DAVIS MUNCK, A PROFESSIONAL CORPORATION

## ACCOUNT DETAIL REPORT

Date Range
From 10/7/2003 0:00
To 10/7/2003 23:59

Disb Transaction(s)

| User Name | Date | Time | Unit ID | Description | DisbName | Net Charges | Status |
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## ni01-00050 Stmicroelectronics Inc. / Us Pat App Pyramid Adder

Copy Transaction(s)

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| Hamilton Kathy | 10/7/2003 | 16:50 | CFX01 | | Letter | 47 | 9.40 | Billed |
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**als For Stmi01-00050:** 10.69

Mailed: OCT 1, 2003

In re. Application of: William E. Ballachino
Serial No.: 09/667,164
Filing Date: September 21, 2000
Title: M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Docket No.: 00-C-050 (STMI01-00050)

The following documents were received in the U.S. Patent and Trademark Office on the date stamped below:

1) Response Under 37 C.F.R. §1.111; and
2) Certificate of Mailing by First Class Mail

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| Examiner: | Chat C. Do |

MAIL STOP NON-FEE AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Response Under 37 C.F.R. §1.111;
2. Postcard Receipt.

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP NON-FEE AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 7, 2003.

Date: Oct 7, 2003 Kathy Hamilton
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DOCKET NO. 00-C-050 (STMI01-00050) PATENT
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MAIL STOP NON-FEE AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE UNDER 37 C.F.R. §1.111

In response to the Office Action dated July 7, 2003, please amend the above-identified patent application as follows.

## CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive [[s]] a first data bit, $A_X$, from said first M-bit argument and a first data bit, $B_X$, from said second M-bit argument, ~~and~~

generate [[s]] both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$, and

provide the first and second conditional carry-out bits to another of said adder cells,

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

2. (Original) The M-bit adder as set forth in Claim 1 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

3. (Original) The M-bit adder as set forth in Claim 2 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

4. (Original) The M-bit adder as set forth in Claim 3 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

5. (Original) The M-bit adder as set forth in Claim 4 wherein said first row of adder cells further comprises a second adder cell coupled to said least significant adder cell, wherein said second adder cell receives a second data bit, $A_{X+1}$, from said first M-bit argument and a second data bit, $B_{X+1}$, from said second M-bit argument, and receives from said least significant adder cell said $C_X(1)$ bit and said $C_X(0)$ bit.

6. (Original) The M-bit adder as set forth in Claim 5 wherein said second adder cell generates a first conditional carry-out bit, $C_{X+1}(1)$, wherein said $C_{X+1}(1)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(1)$ bit from said least significant adder cell.

7. (Original) The M-bit adder as set forth in Claim 6 wherein said second adder cell generates a second conditional carry-out bit, $C_{X+1}(0)$, wherein said $C_{X+1}(0)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(0)$ bit from said least significant adder cell.

8. (Original) The M-bit adder as set forth in Claim 7 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(1)$ bit from said least significant adder cell.

9. (Original) The M-bit adder as set forth in Claim 8 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(0)$ bit from said least significant adder cell.

10. (Original) The M-bit adder as set forth in Claim 9 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

11. (Original) The M-bit adder as set forth in Claim 1 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

12. (Currently Amended) A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline, wherein at least one of said N processing stages comprises an M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit, said M-bit adder comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive [[s]] a first data bit, $A_X$, from said first M-bit argument and a first data bit, $B_X$, from said second M-bit argument, ~~and~~

generate [[s]] both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$, and

provide the first and second conditional carry-out bits to another of said adder cells,

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

13. (Original) The data processor as set forth in Claim 12 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

14. (Original) The data processor as set forth in Claim 13 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

15. (Original) The data processor as set forth in Claim 14 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

16. (Original) The data processor as set forth in Claim 15 wherein said first row of adder cells further comprises a second adder cell coupled to said least significant adder cell, wherein said second adder cell receives a second data bit, $A_{X+1}$, from said first M-bit argument and a second data bit, $B_{X+1}$, from said second M-bit argument, and receives from said least significant adder cell said $C_X(1)$ bit and said $C_X(0)$ bit.

17. (Original) The data processor as set forth in Claim 16 wherein said second adder cell generates a first conditional carry-out bit, $C_{X+1}(1)$, wherein said $C_{X+1}(1)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(1)$ bit from said least significant adder cell.

18. (Original) The data processor as set forth in Claim 17 wherein said second adder cell generates a second conditional carry-out bit, $C_{X+1}(0)$, wherein said $C_{X+1}(0)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(0)$ bit from said least significant adder cell.

19. (Original) The data processor as set forth in Claim 18 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(1)$ bit from said least significant adder cell.

20. (Original) The data processor as set forth in Claim 19 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said $A_{X+1}$ data bit, said $B_{X+1}$ data bit, and said $C_X(0)$ bit from said least significant adder cell.

21. (Original) The data processor as set forth in Claim 20 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

22. (Original) The data processor as set forth in Claim 12 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

23. (Original) A method of adding a first M-bit argument and a second M-bit argument in an M-bit adder, the M-bit adder comprising M adder cells arranged in R rows, the method comprising the steps of:

receiving a first data bit, $A_X$, from the first M-bit argument and a first data bit, $B_X$, from the second M-bit argument in a least significant adder cell in a first one of the rows of adder cells;

calculating in the least significant adder cell a first conditional carry-out bit, $C_X(1)$, assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1;

calculating in the least significant adder cell a second conditional carry-out bit, $C_X(0)$, assuming the row carry-out bit from the second row is a 0;

calculating in the least significant adder cell a first conditional sum bit, $S_X(1)$, assuming the row carry-out bit from the second row is a 1;

calculating in the least significant adder cell a second conditional sum bit, $S_X(0)$, assuming the row carry-out bit from the second row is a 0;

propagating the $C_X(1)$ bit and the $C_X(0)$ bit to a second adder cell in the first row of adder cells; and

selecting one of the $S_X(1)$ bit and the $S_X(0)$ bit to be output from the least significant adder cell according to a value of the row carry-out bit from the second row.

## REMARKS

Claim 1-23 were pending in this application.

Claims 1-23 have been rejected.

Claims 1 and 12 have been amended as shown above.

Claims 1-23 remain pending in this application.

Reconsideration and full allowance of Claims 1-23 are respectfully requested.

## I. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-23 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,682,303 to Uya ("*Uya*"). The Office Action also rejects Claims 1-10, 12-21, and 23 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,852,568 to Ranjan ("*Ranjan*"). These rejections are respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

*Uya* recites a parallel binary adder that includes a series of block-adders. (*Col. 1, Lines 59-62*). Each block-adder includes a first adder for adding arguments assuming "carry input data" equals one and a second adder for adding arguments assuming the "carry input data"

equals zero. (*Col. 1, Line 59 - Col. 2, Line 6*). Each of the first and second adders generates a sum and a carry-out value. (*Col. 3, Lines 31-42*). The results (sum and carry-out) from one of the two adders is then selected and output based on an input from a previous block-adder. (*Col. 2, Lines 7-11*).

*Uya* simply recites the use of multiple adders in a block-adder, where each adder generates a single sum and a single carry-out value. The sum and carry-out from one of the adders is then selected and sent to another block-adder. *Uya* lacks any mention of providing both carry-out values produced by both adders to another block-adder. In particular, *Uya* lacks any mention of an "adder cell" that is operable to "provide the first and second conditional carry-out bits to another of said adder cells" as recited in Claims 1 and 12. *Uya* also lacks any mention of "propagating the $C_X(1)$ bit [a first conditional carry-out bit] and the $C_X(0)$ bit [a second conditional carry-out bit] to a second adder cell in the first row of adder cells" as recited in Claim 23. As a result, *Uya* fails to anticipate all elements of Claims 1, 12, and 23.

For these reasons, the Office Action does not show that *Uya* anticipates the Applicant's invention recited in Claims 1, 12, and 23 (and their dependent claims).

*Ranjan* recites an adder system that includes one or more adder block subsystems. (*Abstract*). Each adder block subsystem includes an adder circuit block, which includes a conditional sum-select circuit and a conditional carry-select circuit. (*Col. 5, Lines 18-25*). The conditional sum-select circuit includes logic adders (elements 395a-395h). (*Col. 7, Lines 63-65*). The conditional carry-select circuit includes logic OR subcircuits (elements 440a-440h) and logic AND subcircuits (elements 450a-450h). (*Col. 9, Lines 52-53*).

The Office Action does not identify the specific components in *Ranjan* relied upon as anticipating the "adder cells" of Claims 1, 12, and 23. The only adders in *Ranjan* are the logic adders, which clearly do not "generate both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$" and "provide the first and second conditional carry-out bits to another of said adder cells" as recited in Claims 1 and 12. The logic adders of *Ranjan* also are not capable of "propagating the $C_X(1)$ bit and the $C_X(0)$ bit to a second adder cell in the first row of adder cells" as recited in Claim 23.

For these reasons, the Office Action does not show that *Ranjan* anticipates the Applicant's invention recited in Claims 1, 12, and 23 (and their dependent claims).

Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejections and full allowance of Claims 1-23.

## II. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 11 and 22 under 35 U.S.C. § 103(a) as being unpatentable over *Ranjan* in view of U.S. Patent No. 4,623,982 to Ware ("*Ware*"). This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re*

*Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

As described above, the Office Action does not show that *Ranjan* recites particular elements of Claims 1 and 12. *Ware* is cited by the Office Action only as showing a particular arrangement of adder cells. *Ware* is not cited by the Office Action as disclosing, teaching, or

suggesting any elements of Claims 1 and 12. As a result, the Office Action does not show that the proposed *Ranjan-Ware* combination discloses, teaches, or suggests all elements of Claims 1 and 12 (and therefore Claim 11 depending from Claim 1 and Claim 22 depending from Claim 12).

Accordingly, the Applicant respectfully requests withdrawal of the § 103(a) rejection and full allowance of Claims 11 and 22.

## III. CONCLUSION

As a result of the foregoing, the Applicant asserts that all pending claims in the application are in condition for allowance and respectfully requests an early allowance of such claims.

## SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Davis Munck Deposit Account No. 50-0208. No extension of time is believed to be necessary. If an extension of time is needed, however, the extension is requested. Please charge the fee for the extension to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: October 7, 2003

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